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NULLED ERROR AMPLIFIER

Field of the Invention

The present invention is related to a method and system for reducing offset related errors in a voltage reference circuit. More particularly, the present invention is related to an array of amplifiers that are configured to minimize the effects of offset voltages in a voltage reference circuit.

Background of the Invention

Band-gap voltage references are used as voltage references in electronic systems. The energy band-gap of Silicon is on the order of 1.2V, and is independent from temperature and power-supply variations. Bipolar transistors have a negative temperature drift with respect to their base-emitter voltage (Vbe decreases as operating temperature increases on the order of -2mV/deg C). However, the thermal voltage of a bipolar transistor has a positive temperature drift (Vt = kT/q, thus Vt increases as temperature increases). The positive temperature drift in the thermal voltage (Vt) may be arranged to compensate the negative temperature drift in the bipolar transistor's base-emitter voltage. Band-gap reference circuits use the inherent characteristics of bipolar transistors to compensate for temperature effects and provide a stable operating voltage over various power-supply and temperature ranges.

An example band-gap reference circuit is illustrated in FIGURE 6. As shown in the figure, two bipolar transistors (Q61, Q62) are arranged with a common base. Two resistors (R61, R62) are series connected between the emitter of the first bipolar transistor (Q61) and the reference output. Another resistor (R63) is connected between the emitter of the second bipolar transistor and the reference output. An error amplifier (EAMP) is used to adjust the voltage of the reference output (VREF) via transistor MLDO. At steady-state, the voltage at the common point of resistors R61 and R62 is the same as the voltage at the emitter of the second bipolar transistor (Q65). The two bipolar transistors (Q61, Q62) are arranged to provide a ten-to-one (10:1) current

density difference with respect to one another. The ten-to-one current density results in a 60mV difference between the base-emitter voltages of two bipolar transistors ($\Delta Vbe = Vt*\ln(I1/I2) = 26mV*\ln(10) = 60mV$, at room temperature). The 60mV difference appears across the first resistor (R61). The voltage between the drain of transistor MLDO and ground provides a voltage reference (VREF) that is given as $VREF = Vbe + X*Vt$, where X is a constant that is used to scale the temperature correction factor. The temperature correction factor (X) is adjusted by the ratio of the resistors. Typical temperature corrected reference voltages of 1.25V are achieved by this configuration.

Brief Description of the Drawings

Non-limiting and non-exhaustive embodiments of the present invention are described with reference to the following drawings.

FIGURES 1 - 5 are illustrative schematic diagrams for circuits that are each arranged in accordance with an embodiment of the present invention.

FIGURE 6 is an illustrative schematic diagram for a conventional band-gap reference circuit.

Detailed Description of the Preferred Embodiment

Various embodiments of the present invention will be described in detail with reference to the drawings, where like reference numerals represent like parts and assemblies throughout the several views. Reference to various embodiments does not limit the scope of the invention, which is limited only by the scope of the claims attached hereto. Additionally, any examples set forth in this specification are not intended to be limiting and merely set forth some of the many possible embodiments for the claimed invention.

Throughout the specification and claims, the following terms take at least the meanings explicitly associated herein, unless the context clearly dictates otherwise. The meaning of "a," "an," and "the" includes plural reference. The meaning of "in" includes "in" and "on." The term "connected" means a direct connection between the items connected, without any intermediate devices. The term "coupled" refers to

both direct connections between the items connected, and indirect connections through one or more intermediary items. The term "circuit" may refer to both single components, and to a multiplicity of components. The term component refers to one or more items that are configured to provide a desired function. The term "signal" includes signals such as currents, voltages, charges, logic signals, data signals, optical signals, electromagnetic waves, as well as others. Referring to the drawings, like numbers indicate like parts throughout the views.

Briefly stated, the present invention is related to a multi-stage amplifier circuit that is arranged to minimize offset related errors (e.g., input referred offset voltage) in a reference circuit. The first stage circuit includes an array of amplifier circuits that receive feedback signals. The outputs of the first stage amplifier circuits are coupled together to a common node. The second stage circuit is also coupled to the common node, and arranged to drive a feedback circuit to generate the feedback signals. In one example, the feedback circuit includes a band-gap core. The second stage circuit can be arranged as part of a low-drop out (LDO) regulator. Each of the amplifier circuits in the first stage can be nulled in response to null control signals from a null control logic circuit. The overall offset in the resulting reference circuit is reduced by the selective nulling of the arrayed amplifiers in the first stage circuit.

FIGURE 1 is an illustrative schematic diagram for a circuit (100) that is arranged in accordance with an embodiment of the present invention. Circuit 100 includes a first stage circuit (X1), a second stage circuit (X2), a feedback circuit (X3), and a null control logic circuit (X4).

The first stage circuit (X1) is arranged to receive a feedback signal (FB), a reference signal (REF), and an output signal to a common node. Offset errors in the first stage circuit is selectively nulled by the null control logic circuit (X4) via a set of control signals (e.g., NULL1 through NULLN). The second stage circuit is arranged to receive an input signal from the common node, and also arranged to provide a reference voltage (VREF1) to an output node (OUT). The feedback circuit (X3) is arranged to provide one or more feedback signals (e.g., FB) in response to the reference voltage (VREF1).

First stage circuit X1 includes an array (N) of amplifier circuits that are denoted as amplifier circuits A1 through AN. Each of the amplifier circuits (A1 through AN) includes three inputs and an output. Each of the first inputs is coupled to the feedback signal (FB). Each of the second inputs is coupled to the reference signal (REF) or another feedback signal (e.g., see FIGURES 2 – 5). Each of the third inputs is coupled to a respective one of the set null control signals (NULL1 through NULLN). Each of the outputs is coupled to the common node. Second stage circuit X2 may include one or more functional blocks. For example, a second stage amplifier circuit may be coupled to an output circuit as shown in FIGURE 1. Feedback circuit X3 may be implemented as a voltage divider circuit, a buffer circuit, a source follower circuit, a band-gap core circuit, another amplifier circuit, and/or a combination of other circuits that provide a feedback signal in response to the output signal.

Conventional reference circuits such as that depicted in FIGURE 6 require some sort of trimming mechanism to adjust the reference voltage (VREF) to a maximally flat response over a specified temperature range. The trimming can be accomplished by adjusting the resistor values in the band-gap core. The trimming in conventional band-gap reference circuits is predominately done to eliminate the mismatch variations in the diode devices (Q61, Q62).

When trimming band-gap references it is often hard to find the appropriate reference voltage for trimming because the absolute value of the optimal reference voltage varies from device to device. The voltage variation is not necessarily due to the mismatch in resistor values or diode devices, but instead is dramatically impacted by offset voltages in the error amplifier (e.g., EAMP). A significant problem that has been observed in addressing the present invention is a phenomenon of assembly related shifts in the reference circuit due to thermal and mechanical stresses on the devices when packaged. For example, a semiconductor die is typically attached to a lead frame in a package where a molding compound is injected over the surface of the die. For this example, the thermal expansion coefficients associated with the molding compound is typically greater than that of the die. The shifts in the reference circuit are

predominately the result of variations in the offset in the error amplifier and shifts in resistor values.

Adjustments to the reference voltage in the circuit are typically done by wafer probing, and trimming prior to packaging the device. The adjustments can be lost based on the aforementioned shifts as a result of the mechanical packaging and assembly process. Moreover, the error amplifier and band-gap core circuits may have non-canceling temperature coefficients. Since the temperature coefficients of the offset voltages are likely different, the temperature related drift characteristics that are achieved by trimming the offset voltage at room temperature may be less than ideal.

The present invention addresses the error amplifier offsets using an array of nulled amplifiers as illustrated in FIGURES 1 through 5. Each amplifier (A1 – AN) in the first stage circuit is basically a trans-conductance (or gm) cell. The outputs of each of the amplifiers in the first stage circuit are combined at a common node. The common node is used as an input to the second stage circuit, which drives the feedback circuit to provide feedback signals for closed loop operation. By combining a number (N) of amplifiers in parallel, the sigma of the offset based error for the error amplifier (the combined array of amplifiers) corresponds to the offset of an individual amplifier divided by the square root of N. The wideband and 1/f noise are also reduced in the same manner. Switching noise due to the nulling operation is very low, providing a suitable solution for low noise LDO, switching regulator, and voltage reference applications.

The null control logic (X4) is arranged to control the nulling operation for each of the amplifiers via control signal NULL1 through NULLN. The nulling operation for a selected amplifier circuit is accomplished by zeroing one of the selected amplifiers in an "off-line" procedure (see FIGURE 4 and related discussion). Examples of nulling and the sequencing of the nulling procedure will be described later.

FIGURE 2 illustrates another circuit (200) that is arranged according to an embodiment of the present invention. The example illustrated in FIGURE 2 is substantially similar to the example illustrated in FIGURE 1. The second stage circuit (X2) in FIGURE 2 is illustrated as a current source (IS2) and a p-type output transistor

(MP2), while the feedback circuit (X3) is illustrated as a band-gap core circuit that includes two output signals (FB1, FB2). A compensation capacitor (CC2) is used to miller compensate the circuit for stability. The null control logic circuit (X4) in FIGURE 2 includes a barrel shifter (X21) that is responsive to a clock signal (CLK) to provide the control signals (NULL1 – NULLN).

FIGURE 3 illustrates yet another circuit (300) that is arranged according to an embodiment of the present invention. The example illustrated in FIGURE 3 is substantially similar to the example illustrated in FIGURE 2. The second stage circuit (X2) in FIGURE 3 is illustrated as a current source (IS3) and an n-type output transistor (MN3), while the feedback circuit (X3) is illustrated as a band-gap core circuit that includes two output signals (FB1, FB2). A compensation capacitor (CC3) is used to miller compensate the circuit for stability. The null control logic circuit (X4) in FIGURE 3 includes a counter (X31) that is responsive to a clock signal (CLK), and a decoder (X32) that are arranged to provide the control signals (NULL1 – NULLN).

FIGURE 4 illustrates still another circuit (400) that is arranged according to an embodiment of the present invention. Circuit 400 includes a first stage circuit (X1), a second stage circuit (X2), a feedback circuit (X3), and a null control logic circuit (X4).

The first stage circuit (X1) includes is arranged to receive two feedback signals (FB1, FB2), and provides an intermediate signal at a common node (N4). The second stage circuit (X2) is arranged to provide an output signal (VREF4) at output node OUT in response to the intermediate signal from node N4. The feedback circuit (X3) is arranged as a band-gap core circuit that provides feedback signals FB1 and FB2 in response to the output signal. The null control logic circuit (X4) is arranged to provide timing signals (NULL1, NULL1', NULL2, NULL2') for nulling an amplifier in the first stage circuit (X1).

An example amplifier circuit is represented in FIGURE 4 by seven transistors (M1 – M7), six switches that are illustrated by transistors MS1 through MS6, and two capacitors (CZ1, CZ2). Transistor M1 includes a source that is coupled to node N7, a gate that is coupled to node N1, and a drain that is coupled to node N3. Transistor

M2 includes a source that is coupled to node N7, a gate that is coupled to node N2, and a drain that is coupled to node N4. Transistor M3 includes a source that is coupled to VSS, and a gate and drain that are coupled to node N3. Transistor M4 includes a source that is coupled to VSS, a gate that is coupled to node N3, and a drain that is coupled to node N4. Transistor M5 includes a source that is coupled to VDD, a gate that is coupled to a bias signal (BIAS), and a drain that is coupled to node N7. Transistor M6 includes a source that is coupled to VSS, a gate that is coupled to node N6, and a drain that is coupled to node N4. Transistor M7 includes a source that is coupled to VSS, a gate that is coupled to node N5, and a drain that is coupled to node N3. Transistor MS1 includes a source and drain that are coupled between node N1 and feedback signal FB1, and a gate that is coupled to signal NULL1. Transistor MS2 includes a source and drain that are coupled between node N2 and feedback signal FB2, and a gate that is coupled to signal NULL1. Transistor MS3 includes a source and drain that are coupled between node N1 and node N2, and a gate that is coupled to signal NULL1'. Transistor MS4 includes a source and drain that are coupled between node N3 and node N5, and a gate that is coupled to signal NULL2'. Transistor MS5 includes a source and drain that are coupled between node N4 and node N6, and a gate that is coupled to signal NULL2'. Transistor MS6 includes a source and drain that are coupled between node N4 and N11, and a gate that is coupled to signal NULL2. Capacitor CZ1 is coupled between node N5 and VSS. Capacitor CZ2 is coupled between node N6 and VSS.

Transistors M1 – M5 are arranged as a trans-conductance cell, where transistor M5 is arranged as a current source, transistors M1 and M2 are arranged as a differential pair, and transistors M3 and M4 are arranged in a current mirror configuration. Transistors MS1, MS2 and MS6 are operated as closed switches when the amplifier circuit is online. When the amplifier circuit is offline, transistors MS1 and MS2 operate as open switches such that the feedback signals are isolated from the input of the differential pair. Similarly, the output of the amplifier circuit is isolated from loading down the other on-line amplifiers by operating transistor MS6 as an open switch when the amplifier circuit is offline.

During one zeroing phase, nulling signal NULL1 is deasserted such that transistors MS1 and MS2 are operated as an open circuit switch that isolates signals FB1 and FB2 from nodes N1 and N2, respectively. During another zeroing phase, signal NULL1' is asserted such that transistor MS3 is operated as closed switch where the inputs of the differential pair are coupled together. Nulling signals NULL1 and NULL1' are preferably arranged for non-overlapping operation such that the inputs of the differential pair are shorted together after the feedback signals (FB1, FB2) are isolated from the differential pair at nodes N1 and N2. For the example illustrated in FIGURE 4, transistors MS1 and MS2 are preferably matched to one another so that their switching operation results in charge injection effects and glitch effects that are matched on both signal lines (FB1, FB2). The remaining online amplifier circuits will reject the matched glitches since they are common-mode signals.

During still another zeroing phase, nulling signal NULL2 is deasserted such that transistor MS6 is operated as an open switch when off-line. During yet another zeroing phase, transistors MS4 and MS5 are operated as closed switches such that transistor MS4 configures transistor M7 to operate as a diode and MS5 configures transistor M6 to operate as another diode. Capacitors CZ1 and CZ2 store the zero condition such that the amplifier is nulled. Nulling signals NULL2 and NULL2' are preferably arranged for non-overlapping operation such that the output of the amplifier circuit is isolated from the other on-line amplifiers before the nulling operation is performed.

The band-gap core circuit (X3) is represented by two p-type transistors (Q1, Q2) and three resistors (R1 – R3). Transistor Q1 includes a collector that is coupled to VSS, a base and emitter that are coupled to node N8, and has an effective area corresponding to nX. Transistor Q2 includes a collector that is coupled to VSS, a base and emitter that are coupled to node N9, and has an effective area corresponding to X. Resistor R1 is coupled between node N8 and node N10. Resistor R2 is coupled between node N10 and OUT. Resistor R3 is coupled between node N9 and OUT. Node N10 is associated with the first feedback signal (FB1), while node N9 is associated with the second feedback signal (FB2).

FIGURE 5 illustrates yet another circuit (500) that is arranged according to an embodiment of the present invention. Circuit 500 includes a first stage circuit that is represented as an amplifier (AMP), a second stage circuit that is represented by transistor MPO and current source transistor MNS, and a feedback circuit that is represented as a band-gap core. The operation of circuit 500 is substantially similar to that described with respect to FIGURES 1 through 4 previously.

An example nulling procedure can be implemented by selecting each of the amplifiers in turn. Each amplifier circuit that is selected is initialized to a nulled condition such that the offset is zeroed out. After every one of the amplifiers is taken offline, the cycle repeats such that the overall offset in the system is zero. This example nulling procedure can be implemented with a null logic circuit that includes a shift register such as a barrel shifter as illustrated in FIGURE 2, a counter and a decoder as illustrated in FIGURE 3, or any other appropriate sequencing logic circuit. An example offset nulling sequence for a set of four amplifiers is illustrated below with offsets corresponding to +2mV, +1mV, -3mV, and -2mV, respectively.

Time	Offset A1	Offset A2	Offset A3	Offset A4	Avg Offset
t0	+2.0mV	+1.0mV	-3.0mV	-2.0mV	-0.50mV
t1	0.0mV	+1.0mV	-3.0mV	-2.0mV	-1.00mV
t2	0.0mV	0.0mV	-3.0mV	-2.0mV	-1.25mV
t3	0.0mV	0.0mV	0.0mV	-2.0mV	-0.5mV
t4	0.0mV	0.0mV	0.0mV	0.0mV	0.0mV

As described above, a shift register (e.g., a barrel shifter) or a counter and decoder can be used in the null control logic to cycle through the amplifiers for nulling each one in turn. In another example, each of the amplifiers is nulled during a power-on-reset (POR) sequence. In still another exampled every other amplifier is nulled in sequence over time. A clock signal or a free running oscillator can be used to synchronize timing in the null control logic circuit (X4).

Another example nulling procedure for four amplifiers is described below, where the amplifiers offsets initially correspond to +2mV, +1mV, -3mV, and -2mV, respectively. For this example, one amplifier (i.e., the seed amplifier) is initially zeroed out so that the average offset that asymptotically approaches zero.

Time	Offset A1	Offset A2	Offset A3	Offset A4	Avg Offset
t0	+2.0mV	+1.0mV	-3.0mV	-2.0mV	-0.50mV
t1	0.0mV	+1.0mV	-3.0mV	-2.0mV	-1.00mV
t2	0.0mV	-1.0mV	-3.0mV	-2.0mV	-1.50mV
t3	0.0mV	-1.0mV	-1.5mV	-2.0mV	-1.25mV
t4	0.0mV	-1.0mV	-1.5mV	-1.25mV	-0.94mV

The above description illustrates an example of how the average offset of the amplifiers might be nulled. For this example, the seed amplifier is initially zeroed at time t1. As time progresses, the average offset associated with the array of amplifiers asymptotically approaches zero. However, one amplifier is taken offline at any given time so that glitches in the system are minimized.

Other example null control logic arrangements are considered within the scope of the present invention. For example, a randomizer can be used to randomly null amplifiers such that the spectrum of the switching noise is spread over many frequencies.

The above specification, examples and data provide a complete description of the manufacture and use of the composition of the invention. Since many embodiments of the invention can be made without departing from the spirit and scope of the invention, the invention resides in the claims hereinafter appended.